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Design and simulation of universal gate using SLM and Savart Plate

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Abstract
The development of science and technology in the last century, have generated a large demand for handling huge volume of data at high speed. To process such enormous data at a high speed, both ultra-high speed processing systems and novel approaches in processing techniques are required. In this paper we have designed and implemented Optical New Quadruple Universal Gate (QUG) using Spatial Light Modulator (SLM) and Savart Plate. We have explained their principle of operations and used a theoretical model to fulfill this task, finally confirming through logical simulations.

Keywords: multi valued logic (MVL), new quadruple universal gate (QUG), spatial light modulator (SLM), savart plate

1. Introduction

In recent years, the multi-valued logic (MVL) system is becoming highly praised by the scientific community for its' inherent property of handling huge volume of data. The main advantages for optical processors lie in the parallel operation but it is also possible to implement MVL in optical system using the polarization states of light along with its presence or absence also [1, 2]. The carry free operation was also suggested using a modified signed digit [3, 4, 5] or modified trinary [6, 7, 8] system. However, Lukasiewicz [9] who initiated the use of ternary logic based on three states has modified it later with an idea that four states logic is a much better proposition. The quadruple-valued logic (QVL) system using SLM and Savart Plate is already implemented [10, 11, 12]. The light incident on Savart Plate is splitted into two orthogonal components and comes out with a spatial shift between them. The electrically addressable negative SLMs are used for the controlling of two components of input light beam. The nature of the negative SLM is such that it is transparent when there is no electric voltage applied on it and it becomes opaque when an electric voltage is applied on it. The property of positive SLM is just reverse. Hence the input may be considered as in the form of di-bit (two bits) representation. In the implementation of QVL system the different states are represented with a di-bit representation using presence and absence of light of two orthogonal polarization states of light beam. The different states are represented with a di-bit representation using presence and absence of light along with the two orthogonal polarization states of light beam [1].

The available universal gates are NAND and NOR Gates. The NAND gate is already implemented by SOA-based Mach–Zehnder interferometer (MZI) [13]. A new universal gate named as NAND has been already designed and implemented [14]. All the above mentioned optical gates provide high speed operation but they cannot handle huge volume of data due to representation in binary domain. With this aim, in this paper we have presented Optical New Quadruple Universal Gate (QUG) using SLM and Savart Plate. As it is a universal gate so all the basic quadruple logic gates are implemented using this QUG in this paper also. The superiority of the proposed scheme is verified by simulation results.

2. Optical New Quadruple Universal Gate (QUG)

The proposed new quadruple universal gate is shown in the Fig 1. By using this gate we can easily implement the operation of all other logic gates like NOT, AND, OR, NAND, NOR, XOR and XNOR.

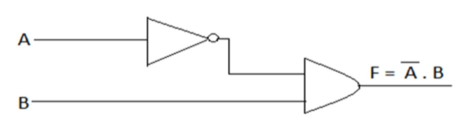

Fig 1: Basic diagram of New Quadruple Universal Gate

Here we are considering A and B as inputs of our proposed new QUG and F= $\bar{A}$.B as the output. The diagrammatic representation of the gate is shown in the Fig 2.

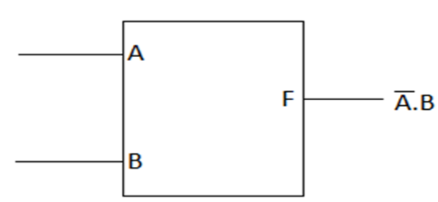

Fig 2: Block diagram of New Quadruple Universal Gate

Now, we are going to implement the new quadruple universal gate optically using SLM (Spatial Light Modulator) and Savart plate. Here the input A is considered in its di-bit form as A_1 and A_2 and B as B_1 and B_2. The New Quadruple Universal Gate has been optically synthesized in Fig 3. In the circuit the Savart plates S_1,S_2,S_3,S_4 and S_5 form the NOT gate and Savart plates S_7,S_8,S_9 and S_{10} constitute the AND gate.

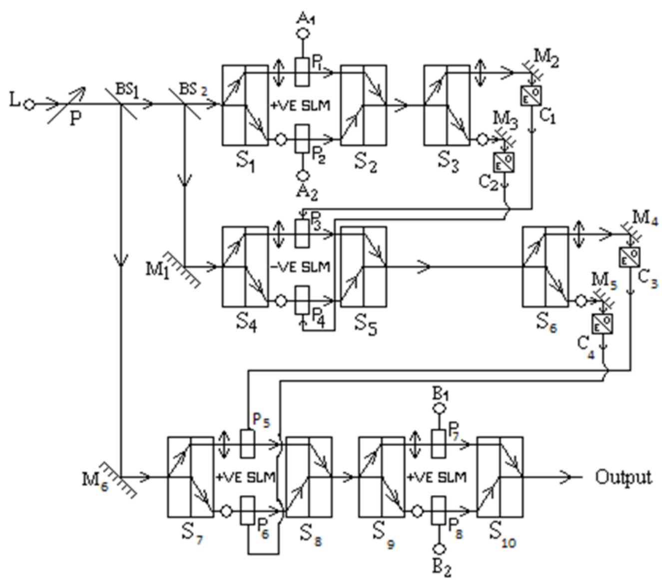

Fig 3: Optical New Quadruple Universal Gate

3. Implementation of Different Quadruple Logic Gates using New Quadruple universal Gate

A gate is said to be universal gate if any basic logic gate can be implemented using this gate. In this section all the basic quadruple logic gates are implemented using the Optical New Quadruple Universal Gate.

3.1 Implementation of Quadruple NOT Gate

Quadruple NOT gate using the new quadruple universal gate is shown in the Fig. 4. Here, we are considering X (X_1, X_2) as one input and the other input is 3(1, 1). The NOT gate gives the output $\overline{X}$ or the complement of the input X.

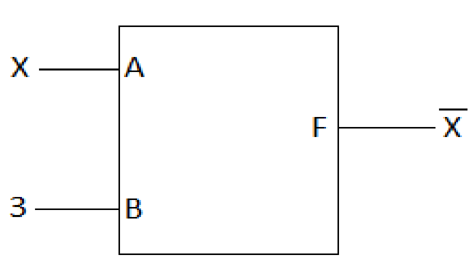

Fig 4: Block diagram of Quadruple NOT gate using New Quadruple Universal Gate

The truth table for the Quadruple NOT gate for all the possible combinations of the input X is shown in the Table 1.

Table 1: Truth table of Quadruple NOT gate using New Quadruple Universal Gate

Inputs						Outputs		
X	**X_1**	**X_2**	**Y**	**Y_1**	**Y_2**	**F_1**	**F_2**	**F**
0	0	0	3	1	1	1	1	3
0	0	0	3	1	1	1	1	3
0	0	0	3	1	1	1	1	3
0	0	0	3	1	1	1	1	3
1	0	1	3	1	1	1	0	2
1	0	1	3	1	1	1	0	2
1	0	1	3	1	1	1	0	2
1	0	1	3	1	1	1	0	2
2	1	0	3	1	1	0	1	1
2	1	0	3	1	1	0	1	1
2	1	0	3	1	1	0	1	1
2	1	0	3	1	1	0	1	1
3	1	1	3	1	1	0	0	0
3	1	1	3	1	1	0	0	0
3	1	1	3	1	1	0	0	0
3	1	1	3	1	1	0	0	0

Now, we are going to represent quadruple NOT gate using the New Quadruple Universal Gate optically by using SLM and Savart plates as shown in Fig. 5.

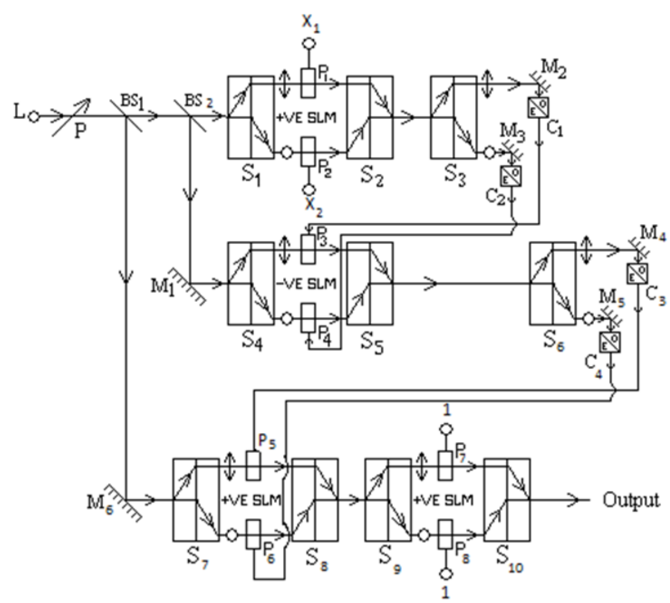

Fig 5: Optical Quadruple NOT gate using New Quadruple Universal Gate

From Fig. 5, we can see that, the NOT gate works on same principle as the basic block of the universal gate except that an input of 3 (1, 1) or high voltages are given to the positive SLMs- P_7 and P_8respectively. Hence the Output is controlled only by the input X (X_1, X_2).

When X= 3 (X_1 = 1, X_2 = 1), then there will be no light at the final output i.e. F=0(F_1 = 0, F_2 =0).

Similarly for the other inputs of X, the result can be verified according to Table 1.

3.2 Implementation of Quadruple AND Gate

We are considering X (X_1, X_2) as one of the inputs of the first block and the other input is 3 (1, 1). It gives the output (F_1) of complemented X which is again fed as the first input to the next block. The second input of the second block is Y (Y_1,Y_2). The second block produces the final output $F_2 = X.Y$.

The truth table for the Quadruple AND gate for all the possible combinations of the input X and Y is shown in the Table 2.

Table 2: Truth table of Quadruple AND gate using New Quadruple Universal Gate

Inputs						Output		
X	X_1	X_2	Y	Y_1	Y_2	F_{21}	F_{22}	F_2
0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0
0	0	0	2	1	0	0	0	0
0	0	0	3	1	1	0	0	0
1	0	1	0	0	0	0	0	0
1	0	1	1	0	1	0	1	1
1	0	1	2	1	0	0	0	0
1	0	1	3	1	1	0	1	1
2	1	0	0	0	0	0	0	0
2	1	0	1	0	1	0	0	0
2	1	0	2	1	0	1	0	2
2	1	0	3	1	1	1	0	2
3	1	1	0	0	0	0	0	0
3	1	1	1	0	1	0	1	1
3	1	1	2	1	0	1	0	2
3	1	1	3	1	1	1	1	3

The quadruple AND gate using the new quadruple universal gate has been represented optically in Fig.7.

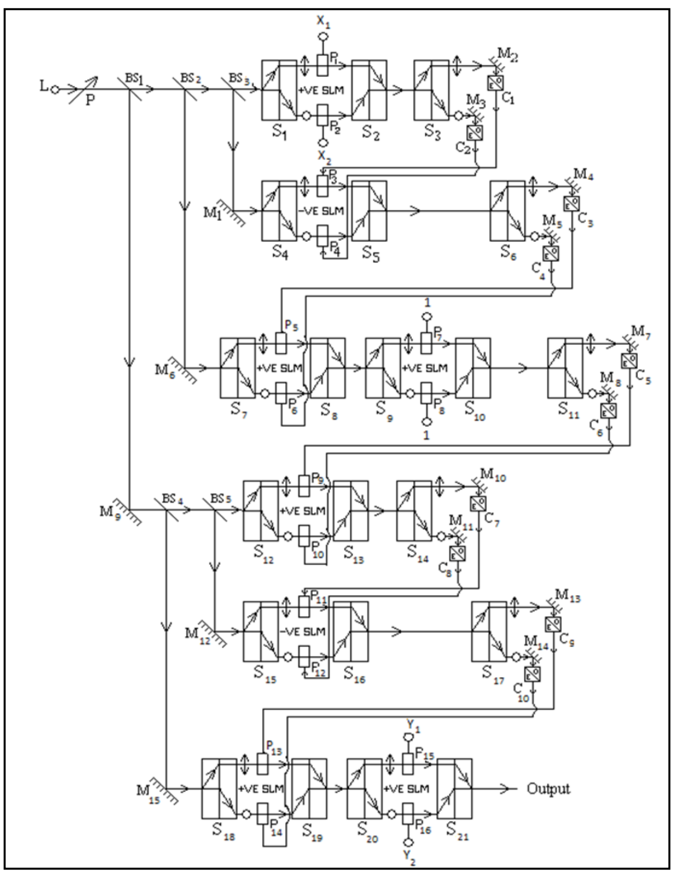

Fig 7: Optical Quadruple AND gate using New Quadruple Universal Gate

For the input X=0 (X_1= 0, X_2= 0) and Y=3 (Y_1=1,Y_2=1) there will be no light present at the final output i.e. F_2=0(F_{21}= 0, F_{22}= 0).

For the input X=2 (X_1= 1, X_2= 0) and Y=2 (Y_1=1, Y_2=0), the final output consists of only horizontally polarized light i.e. F_2=2(F_{21}= 1, F_{22}= 0).

For the input X=3 (X_1= 1, X_2= 1), and Y=1 (Y_1=0, Y_2=1), the final output consists of only vertically polarized light i.e. F_2= 1(F_{21}= 0, F_{22}= 1).

Similarly, for other combinations of inputs X and Y, the results can be verified according to Table 2.

4. Simulation (by matlab7.0) results of the designed gates

The vertical axis in Fig. 8(a) to 8(b) indicates power in dB, while horizontal axis represents time scale in ps. The timing instant for the occurrence of bit pattern is at 1,3,5,7 ps. Upper first two (Fig. 8(a) and Fig. 8(b)) set waveforms indicate the input bit sequences, 0011 and 0101 for the input variables A and B respectively. Similarly, from different output bit patterns gives the different input bit combinations which satisfies the truth tables of all logic gates.

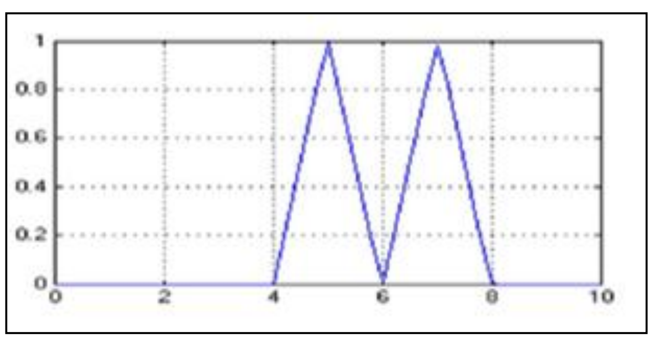

Fig 8a: Input X

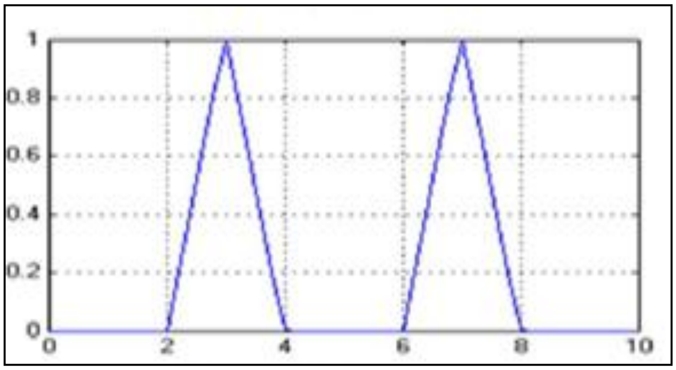

Fig 8b: Input Y

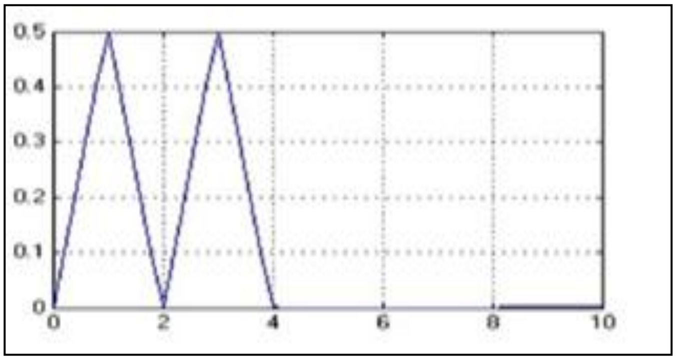

Fig 8c: Output for the NOT operation

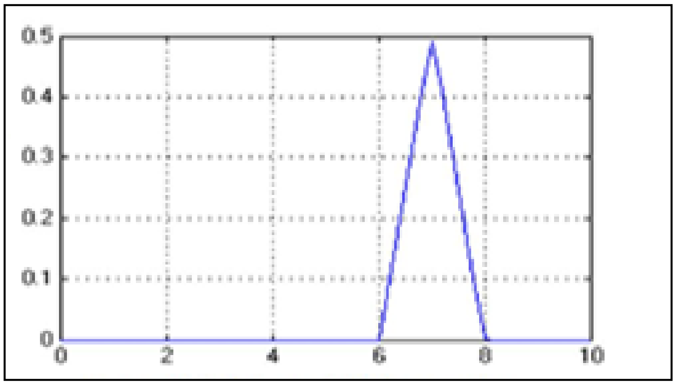

Fig 8d: Output for AND operation

5. Conclusions

In this paper, we have proposed and implemented optical new quadruple universal gate (QUG) along with the realization of the other optical basic logic gates such as NOT and AND gates using this QUG. Simulation result verifies the functionality of those designed gates. The theoretical models developed and the results obtained numerically are useful to future all-optical logic computing system. Different logic operations can easily be achieved with these gates. It has some limitations regarding optoelectronic conversion delays and dense organization of optical processing units, but it also has wide range of applications in complex combinational, sequential circuits as well as in communication fields, optical computational circuitry and artificial intelligence arena.

6. References

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