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# Optimizing performance of an organic field effect transistor

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**Abstract**
The main aim of the present investigation is to study the emerging field of organic electronics and development of new organic field electronic transistors. Performance of an Organic Field Electronic Transistor OFET based on p-type organic semiconductor - poly 3-hexylthiophene (P3HT) in bottom gate bottom contact (BGBC) configuration is analyzed and established optimum processing conditions using various surface treatments. The experiments for fabricating, characterizing and OFET for measuring its performance and improvements with HMDS surface treatment for passivating dangling bonds at dielectric–organic semiconductor interface are studied in this paper. The obtained results are compared with an OFET fabricated without HMDS surface treatment. The HMDS surface treatment makes the gate dielectric ($SiO_2$) hydrophobic from hydrophilic and satisfies dangling bonds at gate dielectric surface, so improves interface for organic semiconductor. With HMDS surface treatment the OFET shows better results like mobility 2.19×10-3 cm2/V-s compared to 8.1×10-4 cm2/V-s for the device without HMDS surface treatment for the device with W/L=24600/70 and for devices with W/L 24300 µm/50µm the improvement was from 9.37 x $10^{-04}$ cm2/V-s to 1.32 x $10^{-03}$ cm2/V-s. This result indicates the OFETs with higher mobility results in better response time and faster operation when used for making organic electronic components based circuits.

**Keywords:** characterization; fabrication; optimization; organic electronics, p-type organic semiconductor

## Introduction
Due to various advantages like low cost and simple processing, flexible substrate and large area coverage, electronic components based on organic semiconducting, conducting and insulating materials are attracting more and more researchers to the field of organic electronics. Based on the literature survey on organic electronics and processes involved in fabrication of an OFET is developed.

## Field Effect Transistors
The Field Effect Transistor is a three terminal Uni polar Semi conductor device in which Current is controlled by an Electric field.

## Organic Semiconductor
These are based on the unusual properties of the carbon atom among other configurations, the energy difference between occupied orbital and Unoccupied orbital are quite large correspondingly larger chains of bound carbon atom would have large gap between Highest Occupied Molecular Orbital (HOMO) and Lowest Unoccupied Molecular Orbital (LUMO) leading to insulating properties. Common Organic semi conductors are divided into two types they are p-type and n-type. Example for p-type: poly-3hexilthiphene (P3HT), Poly–thenelenevinelene (PVT), pentacene. Examples for n-type: the functionalize

## Organic Field Effect Transistor
A typical OFET is composed of gate electrode, Dielectric layer, Organic Semiconductor layer and Source-Drain(S-D) electrodes. The charge carrier's density in channel between source and drain contacts can be controlled by the applied Gate voltage across a thin dielectric the current is given by:

$$I_{ds}=\frac{1}{2}\mu C_{ox}\frac{W}{L}(Vgs-VT)^2 \quad \ldots\ldots\ldots\ldots\ldots\ldots(1)$$

where µ is the field-effect mobility, Cox is the capacitance per unit area of the gate dielectric [F/cm2], VT is the threshold voltage, and W (width) and L (length) are the dimensions of the semiconductor channel defined by the source and drain electrodes of the transistor.
Organic Field Effect Transistors (OFETs) use organic semiconductor materials rather than inorganic semiconductor materials like Si or Ge for their active material. This active material can be composed of a wide variety of molecules. Depending on the design of the OFET and the specific materials and processes used to manufacture it, the cost and performance of the OFET can vary substantially.

## Most Common Designs
Depending on the position of the gate-bottom or top, and position of Source/drain contacts – bottom or top. There are four different geometrical structures possible for OFETs.

1. Top Gate Structures: a. Top Contacts b. Bottom Contacts.
2. Bottom Gate Structures: c. Top Contacts d. Bottom contacts.

## Top Contact
If the source/drain contacts are on the top of

semiconducting material it is called top contact structure.

- **Bottom Contact:** If the source/drain contacts are below the semiconducting material, it is called bottom contact structure
- **Top Gate Geometry:** When dielectric is grown on top of semiconducting material and gate is placed on the top of the dielectric, the resulting structure is called top gate geometry.
- **Bottom Gate Geometry:** When gate structure is first patterned on the substrate, dielectric material is placed above that and semiconducting material is placed on the top, the resulting structure is called Bottom Gate Geometry.

The experiments were done with bottom gate bottom contact structure of the device which is shown in Figure 1.

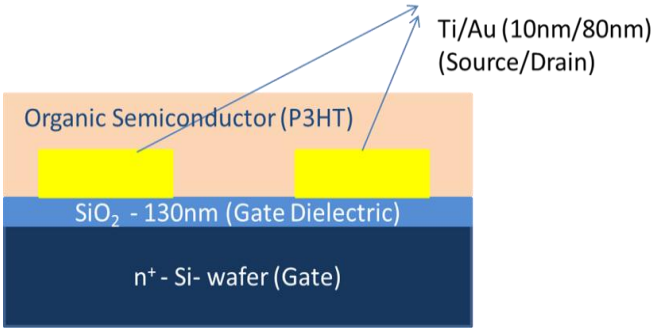


**Fig 1:** Schematic of a Bottom Gate Bottom Contact OFET

## Fabrications

Devices fabricated with different techniques can exhibit varied field-effect properties. Therefore, solution process have been the most widely applied methods to fabricate organic active films Heavily doped n type silicon wafer with resistivity of about 0.01-0.02Ωcm was used as substrate and acts as gate electrode, and $SIO_2$as gate dielectric layer was thermally grown on silicon wafer by wet oxidation after the RCA Cleaning. The thickness of the layer was observed as 137nm by Ellipsometere. The bottom contacts for source and drain with Ti/Au (10 nm/50 nm) deposited on $SiO_2$ layer using lift-off for realizing comb type structures with various W/L ratios. Fabrication of OFET involves following process steps.

## Substrate selection

The substrate with following parameters was used:

- Diameter of Silicon Wafer=2inch highly Doped n-type
- Resistivity =0.01-0.02Ωcm
- Thickness of Wafer=250µm.
- Cristal Orientation=<100>.

## RCA cleaning of Wafer

To make the wafer free of contamination (Organic and metallic) I perform a wafer cleaning performance that is RCA (Radio Corporation of America) RCA involves three steps.

1. Substrate is cleaned in 2 % HF in H2O and then in DI water. Removal of metallic and Organic impurities is done using H2SO4. H2SO4:H2O2 in composition 1:2:7 is used at 90oC for organic contamination & particle removal.
2. Standard Cleaning- 1 (SC- 1) Step: NH4OH+H2O2+H2O in composition1:2:7 at 70-80oC. Removes organic contamination and particles by oxidation
3. Standard Cleaning- 2 (SC- 2) Step: HCl+H2O2+H2O composition at1:2:7 at 70- 80oC, desorbs metal contamination by forming a soluble complex.
4. Buffered HF dip after each of the above processes. First step is done to removal of organic impurities, second step is done for removal of heavy metallic impurities and the third step is for the removal of alkali metals like (Na, Ka,) etc.

## Oxidation

In FET we need to have an insulator layer between the Gate and the bulk.

Use Silicon dioxide as the insulator. On silicon wafer this oxide layer is done by two methods:

- Deposition
- Growth

It has been found that grown oxide has better than deposited one. Oxide growth can be done by two methods:

- Wet oxidation and
- Dry oxidation
- Si+□O2->SiO2 for dry oxidation
- Si□2+H2O->SiO2+□2H2 for wet oxidation
- Dry oxidation provides better than Wet oxidation, wet oxidation is taken in the study.

In case of wet oxidation, the chamber, after being heated up to 1000◦C, is cooled back to around 200-300◦C and then the wafers are unloaded. This method produces oxide layer of thickness 137nm.

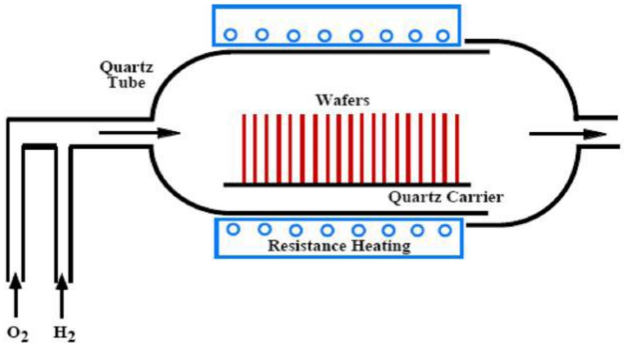


**Fig 2:** Chamber for Oxidation process [9]

The steps for the oxidation process

- The $N_2$ flow is switched on and set to 150ml/min in the outer tube and 35ml/min in the inner tube.
- The furnace is switched on to ramp up the temperature of around 300°Cand then slowly increased to 1000°C
- As the temperature reaches 1000C the inner $N_2$ is turned off and oxygen flow started at same time
- The time for the oxygen flow is calculated on the basis of the thickness required after that time $O_2$ flow is stopped and $N_2$ is started again
- The furnace is allowed to ramp down until it reaches around 300C at which the wafers are unloaded from the furnace.

After Oxidation the thickness of oxide layer on wafer is 137nm.

**Photo Lithography**

Photolithography is the process of transferring geometric shapes on a mask to the Surface of a silicon wafer. Photo resist is applied to the surface of the wafer by 'spin Coating' This is a process where a required thickness of the Photo resist is obtained by Spinning a wafer at a certain speed The thickness is inversely proportional to the spin Speed.

There are two types of photo resists:

- Positive photo resist (PPR)
- Negative photo resist ( NPR)

The resist is exposed to UV light where ever underlining material is to be removed. Exposure to UV light changes the chemical structure of the resist so that it becomes more soluble in the developer. The exposed resist is then washed away by the Developer solution, leaving windows of the bare underlying material.

Exposure of UV light causes the Negative resist to become polymerized, and more difficult to dissolve. Therefore, the negative resister remains on the surface and developer solution removes solution removes only the unexposed portions. Once the mask has been accurately aligned with the pattern on the wafer' surface (Contact Printing), the photo resist is exposed through the pattern on the mask with High intensity ultraviolet light. The resist-coated silicon wafer is brought into physical Contact with the glass photo mask. The wafer is held on a vacuum chuck, and the whole assembly rises until the wafer and mask contact each other. The photo resist is exposed With UV light while the wafer is in contact position with the mask. Because of the contact between the resist and mask, very high resolution is possible in contact printing (e.g. 1-micron features in 0.5 microns of positive resist).

**Metallization RF by Sputtering**

Adhesive property of Gold (Au) poor to Si, so, Chromium (Cr) is used as Adhesive between the two. Au and Cr are placed in two separate boats made of tungsten or molybdenum and kept in the main chamber. The wafer is subjected to a temperature of200 °C for proper deposition. At this temperature and pressure, Cr is first deposited on Si, upon which Au is deposited with the help of resistive heating of the boats by high Current.

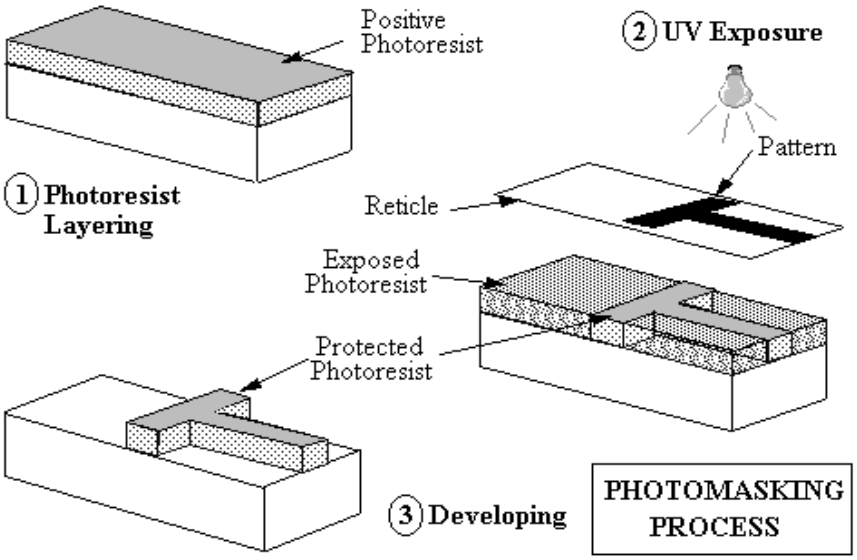


**Fig 3:** Photolithography process [13]

**Organic Semiconductor material Spin coating**

Before spin coating of organic semiconductor material, a process called HMDS treatment is done on the substrate. The mobility of poly (3-hexylthiophene) was found to Vary by two orders of magnitude depending on the solvent used, with chloroform giving the highest mobility. So I prepared solution of 4.75mg of poly (3hexylthiophene) and 1.5 ml of chloroform I tested with and without HMDS. HMDS is placed on the surface of the wafer and wafer is rotated at 4000 rpm for 30 to 40 sec. now, wafer is heated at 120 °C for 5 minutes. So, excess HMDS evaporates from the surface.

For forming layer of organic semiconductor spin coating is the preferred for application of thin, uniform films to flat substrates. An appropriate amount of Polymer solution in chloroform, of the 3 mg/ml chloroform concentration is placed on the Substrate. The substrate is then rotated at speed of 1000 rpm in order to spread the fluid by centrifugal force. Rotation is continued for 45 seconds, with fluid being spun off the Edges of the substrate, until the desired film thickness is achieved. Annealing is then done at 90°C for about 1 hour to remove the organic solvent (chloroform).

**Characterization of Organic Field Effect Transistors**

**Characterization Setup:** The electrical characterization was done in ambient on a probe station using Keithley 2602 SMU and Keithley 236 SMU.

**Characteristics of an Organic Field Effect Transistor**

The key parameters in characterizing a FET are its field effect mobility and on/off ratio. Field-effect mobility

quantifies the average charge carrier drift velocity per unit electric field, whereas on/off ratio is defined as the drain-source current ratio between the "on" and "off" states. Field-effect mobility can be deduced from eq. (1)

$$I_{ds} = (1/2)\ \mu CoxW/L\ (Vgs - V_T)^2 \text{----------} (1)$$

Which describes the drain-source current characteristics in the saturation region of the current-voltage curve as function of gate voltage in eq (1), Where, W = Width of the channel, L = Length of channel Cox = Oxide capacitor per unit area μ = Mobility VT = Threshold voltage Vgs = Gate to source voltage ID = Drain current Here Oxide capacitance per unit area is given by $C=2.66e\text{-}08\ nF/cm^2$

After fabricating the device, W, L and $_{Cox}$ are known. So equation (1) can be rewritten as,

$$\sqrt{Id} = \sqrt{\frac{1}{2}}(\mu C_{ox}/L)(V_{gs}-V_t) \text{ ..... (2)}$$

The slope of line in the saturation region of *ID* vs. $V_{gs}$ can be used to extract mobility μ using above three known terms and $\varepsilon_{ox}$ of the dielectric material. At the same time, the intercept of the line on the x-axis gives the value of the VT-threshold voltage for the fabricated device.

Electrical characteristics of OFETs with, and without HMDS surface treatment were measured and studied for performance improvement. HMDS was spin coated on the surface of the wafer at 4000 rpm 30 to 40 sec. Then the wafer was heated at 120°C for 5 minutes.

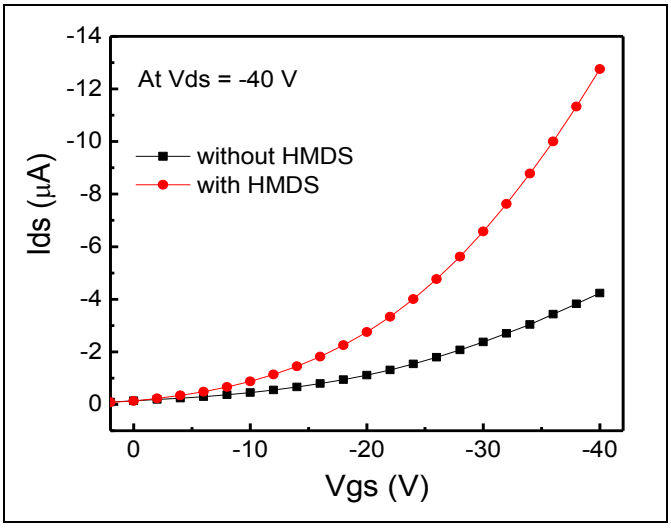


**Fig 4:** $I_DV_G$ characteristics of an OFET with W/L = 24600 μm /70 μm and $t_{ox}$ = 137nm with $V_{DS}$ = -40 V for two devices; one treated with HMDS surface treatment and another without HMDS treatment showing performance improvement in ON current of ~810.097 % and mobility of ~285.11566827% the device with HMDS surface treatment

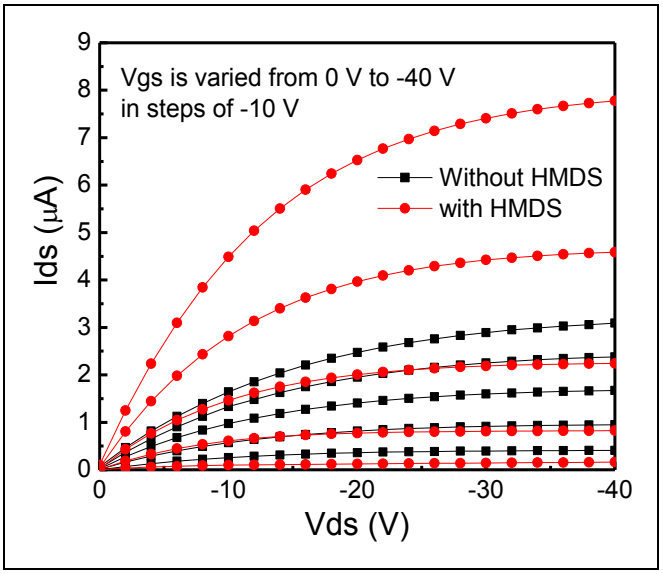


**Fig 5:** $I_DV_D$ characteristics of an OFET with W/L = 24600 μm /70 μm and $t_{ox}$ = 130 nm with $V_{DS}$ varying from 0 V to -40 V in steps of -10 V for two devices; one treated with HMDS surface treatment and another without HMDS treatment showing performance improvement in the device with HMDS surface treatment

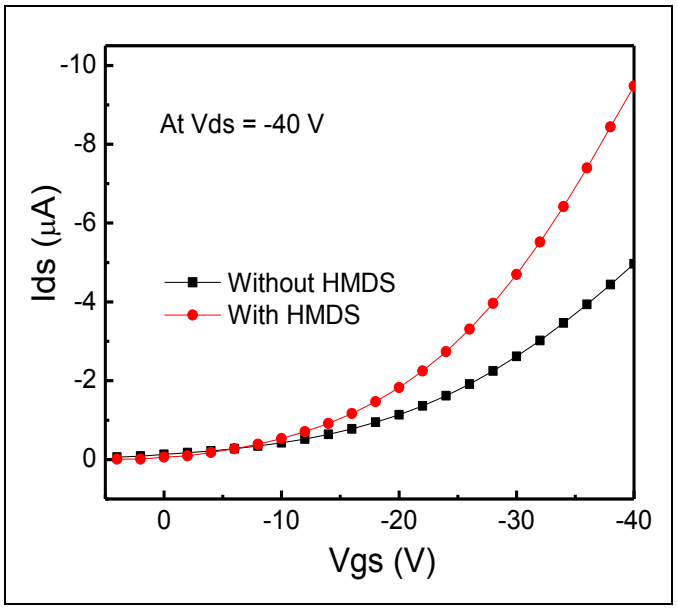


**Fig 6:** $I_DV_G$ characteristics of an OFET with W/L = 24300 μm /50 μm and $t_{ox}$ = 137nm with $V_{DS}$ = -40 V for two devices; one treated with HMDS surface treatment and another without HMDS treatment showing performance improvement in ON current of ~280.18188070% and mobility of ~40.9551727047% the device with HMDS surface treatment

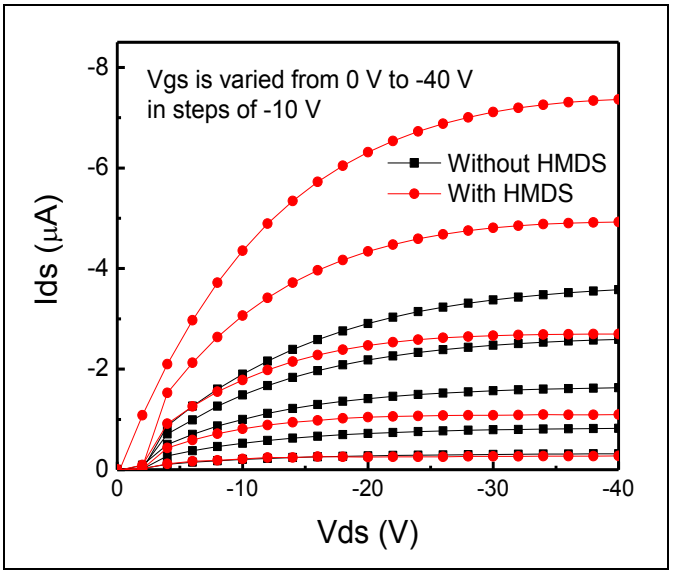


**Fig 7:** $I_DV_D$ characteristics of an OFET with W/L = 24300 µm /50 µm and $t_{ox}$ = 130 nm with $V_{DS}$ varying from 0 V to -40 V in steps of -5 V for two devices; one treated with HMDS surface treatment and another without HMDS treatment showing performance improvement in the device with HMDS surface treatment.

## Experiments and Results

Bottom Gate Bottom Contact (BGBC) device configuration was used for fabrication of OFETs. A highly doped n type silicon substrate acts as gate electrode of the OFET and thermally grown silicon-dioxide ($SiO_2$) of thickness 137nmacts as gate dielectric. Ti/Au layer is patterned using photolithography technique for the source drain electrodes (10 nm/50 nm) in inter digitized configuration.

The experiments reported were performed in two parts. One set of experiments was done in normal ambient conditions with and without HMDS. Here, the substrates are treated with Hexa methyl di silazane (HMDS), by spin coating at 1000 rpm for 10 seconds followed by4000 rpm for 10 seconds. Solutions of 8mgweight were prepared in1.5ml chloroform and spin coated at 500 rpm for 10 seconds followed by 1000 rpm for 30 seconds to give a thin layer (~100 nm) of the blend. The prepared devices are annealed at90 °C for 1 hour. The devices were characterized in normal ambient environment using. The electrical measurements were conducted inside probe station using Keithley2602 SMU and Keithley 236 SMU. All other parameters extracted from IV characteristics of the devices are mentioned in Table 1 and Table 2.

**Table 1:** Various characteristics parameters extracted from $I_DV_G$ characteristics with device details for devices with HMDS surface treatment

| I on | I off | Current Ratio | W | L | $V_{TH}$ | Mobility(µ) |
|---|---|---|---|---|---|---|
| -8.80E-06 | -3.17E-08 | 278 | 24600 | 70 | -8.95 | 1.94E-03 |
| -1.28E-05 | -2.28E-07 | 56 | 24600 | 70 | -2.70 | 2.19E-03 |
| -7.94E-06 | -7.29E-08 | 108 | 24300 | 50 | -6.24 | 1.22E-03 |
| -9.48E-06 | -6.35E-08 | 149 | 24300 | 50 | -6.55 | 1.32E-03 |
| -8.69E-06 | -8.93E-09 | 973 | 24000 | 30 | -8.29 | 8.11E-04 |
| -1.60E-05 | -1.79E-07 | 89 | 24000 | 30 | -6.85 | 1.55E-03 |

**Table 2:** various characteristics parameters extracted from $I_DV_G$ characteristics with device details for devices without HMDS surface treatment

| I on | I off | Current Ratio | W | L | $V_{TH}$ | Mobility(µ) |
|---|---|---|---|---|---|---|
| -4.23E-06 | -1.39E-07 | 30.5025E | 2.46E+04 | 70 | 0.33 | 5.77E-04 |
| -3.47E-06 | -8.75E-08 | 39.7064E | 2.46E+04 | 70 | -1.00 | 5.70E-04 |
| -5.53E-06 | -1.34E-07 | 41.3111E | 2.43E+04 | 50 | -4.58 | 6.80E-04 |
| -9.72E-06 | -2.48E-07 | 39.2565E | 2.43E+04 | 50 | 0.14 | 9.37E-04 |
| -9.72E-06 | -2.48E-07 | 39.1935E | 2.40E+04 | 30 | 0.11 | 5.70E-04 |
| -1.27E-05 | -4.83E-07 | 26.2528E | 2.40E+04 | 30 | 3.39 | 6.36E-04 |

## Results and Discussion

The device with W/L=24600/70 shows a field effect mobility of $2.19\times10^{-3}$ $cm^2$/V-s and the on/off ratios 56. The extracted threshold voltage for this device is -2.70 V. These devices show field effect mobility in the order of $10^{-3}$ $cm^2$/V-s. The devices show good saturation behavior, the characterization was done in ambient conditions. The device shows on/off ratio 56.042. The extracted field effect mobility improved from $8.1\times10^{-4}$ to $2.1\times10^{-3}$ $cm^2$/V-s, showed the performance improvement due to HMDS surface treatment. The percentage of increase in mobility is 285 %. Also, for devices with W/L 24300 µm/50µm the improvement in current ratio was from ~ 40 to.> 110 showing increase of a factor of 2X. The field effect mobility was improved from 9.37E-04 cm2/V-s to 1.32E-03 $cm^2$/V-s.

## Conclusion

The OFETs with higher mobility results in better response time and faster operation when used for making organic electronic components based circuits. This concludes that the OFET with HMDS surface treatment gave better results like mobility when compared the device without HMDS surface treatment.

## Acknowledgements

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## References


1. Karlheinz Bock. Polytronics - Electronics and Systems on Flexible Substrates.
2. Christos D. Dimitrakopoulos and Patrick R. L. Malenfant, Organic Thin Film transistors for Large Area Electronics.
3. Dimitrakopoulos CD, Mascaro DJ. Organic thin-film transistors: A review of recent advances.
4. Prof. Ramgopal Rao V, Saurabh Goyal. Polymers in Electronics (Chapter).
5. Shaw JM, Seidler PF. Organic electronics: Introduction.
6. http://www.ipc.uni-linz.ac.at/os/Organic-Field-effect-transisors-intro.pdf
7. Behrang H, Hamadani, Douglas Natelson. Extracting Contact Effects in
8. Natelson D, Hamadani BH, Ciszek JW, Corley DA, Tour JM. Contact effects in polymer field-effect transistors
9. Plummer Deal, Griffin. Silicon VLSI Technology-Fundamentals, Practice and Modeling: New Delhi: Prentice-Hall Of India, 2000.
10. Dimitrakopoulos CD, Mascaro DJ. Organic thin- D. J Mascaro, Thin film Transistors: A review of recent advances. 2001; 45(1).
11. Shree Prakash Tiwari PhD Thesis, 2008.
12. Harshil N Raval. Polymer Electronics, M. Tech. Seminar Report,
13. Fundamental principles of optical lithography: the science of micro fabrication By Chris Mack.