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Layout designing of full adder with minimum number of transistors using 32nm CMOS technology

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Abstract
Full Adders are the basic and very important component of every circuit and microprocessors. In this paper an efficient and new way of designing the full adders is proposed. Full adder is designed so as to reduce the power consumption and the chip area occupied by it. The proposed design uses 8 Transistors. It is fulfilled by using 2 XNOR (3T+3T) gates and one 2X1 MUX (2T). There are two layouts which have been discussed in this paper. One is auto generated layout and another is customized layout. Both the layouts are compared by taking different parameters like Surf area, power consumption and delay.

Keywords: Layout designing, minimum number, transistors using 32nm

Introduction

Addition is the fundamental arithmetic operation done in system at the elementary level. Full adders are used for the purpose of addition in many VLSI circuit such as application specific DSP architectures, microprocessors, etc. So the performance parameters of the circuit that includes power consumption, chip area, delay depends upon the design of the full adder. Full adder is very important as it is the base of every ALU operation like subtraction, multiplication, division, etc. and it also gives the feature of carry propagation.

The effect of the choice of the design of the full adder is very significant. It is reflected in the form of the performance of the system like its power consumption, time delay, chip area, etc. The power consumption of the full adder depends upon the switching activity and the size of the transistors. The area depends upon the number and size of the transistors. Time delay depends upon the number of transistors and the parasitic capacitance.

Table 1

A	B	C_{in}	Sum	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

In the full adder circuit there are 3 inputs A, B, Cin and the sum is generated by the binary sum of A, B & Cin. Another output Cout is the carry in the summing operation of the 3 inputs.

Both the outputs can be obtained from the following equation:

$SUM = A \oplus B \oplus Cin$

$Cout = A.B + B.C + C.A$

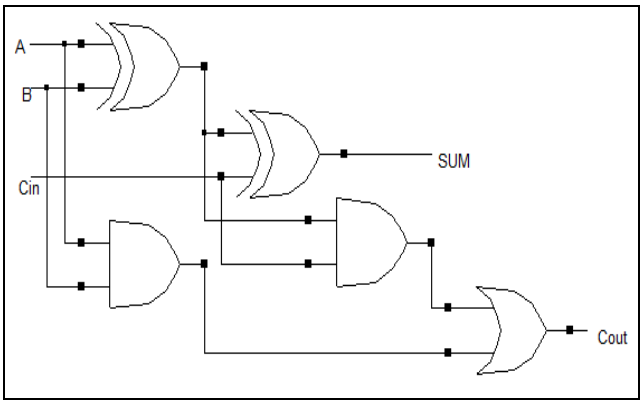

Fig 1: Logic Diagram of Full Adder

The circuit of the full adder can be easily realized by using XOR/XNOR gates and multiplexer. The count of the transistor depends on which type of the design is used for the XOR/XNOR gates and for the multiplexer.

2. Proposed Design

In the proposed design, full adder is realized by using 2 XNOR gates and 1 2x1 MUX. XNOR gates are used to get the Sum and MUX is used to get Cout.

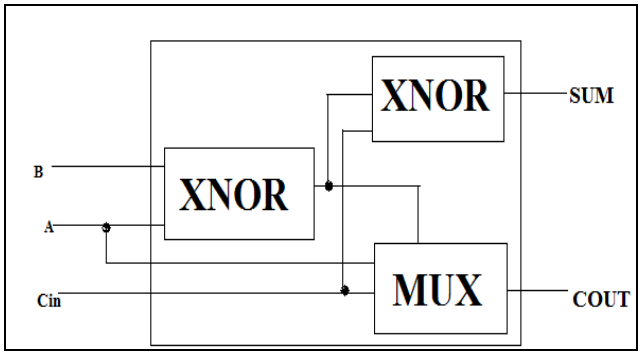

Fig 2: Block Diagram of Proposed Full Adder

XNOR gate is designed using 3T and MUX is designed using 2T.
So total number of transistors is 3T+3T+2T = 8T.

XNOR Design
The proposed diagram of the XNOR gate is shown in the figure:

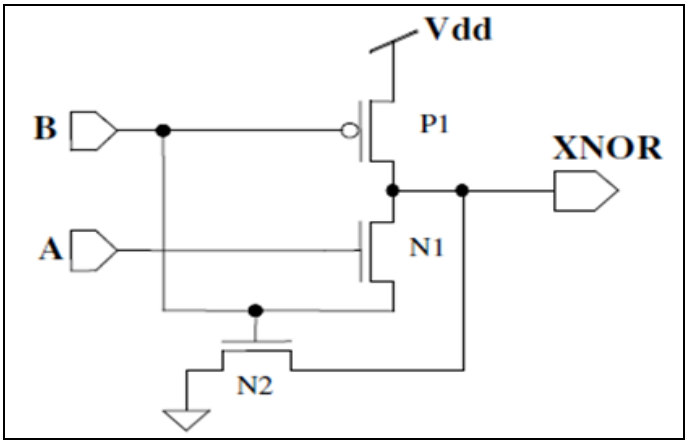

Fig 3: Proposed XNOR cell

XNOR Working
In the proposed XNOR gate 1 PMOS transistor (P1) and 2 NMOS transistors (N1 & N2) are used. The system's behavior for different inputs is described:
For input, A=0 & B=0, P1 will be on and N1 & N2 will be off, so the output will be high as the Vdd is directly going to the output due to on state of P1 and it is not discharged to the ground because no conducting path is present due to off state of N1 & N2.

For A=0 & B=1, P1 & N1 will be off and N2 will be on due to high logic at the gate terminal of N2. So there will be a conducting path present from Output node to ground which discharges it.
For A=1 & B=0, P1, N1 & N2 all will be on. So the output node will be discharged to the ground. P1 will be on and N1 will be on due to their respective inputs and N2 will be on due to conducting path from Vdd to the gate terminal of N2.
For A=1 & B=1, P1 & N2 will be off & N1 will be on, due to which the output node will be high as there is no conducting path from output node to ground. There will be a threshold drop in the N1 and to maintain the high output swing and reduce the threshold voltage drop and to reduce time delay, channel width of N1 can be increased.
There are two XNOR gates which are cascaded to generate the SUM.

MUX Working
Cout is generated by using a 2X1 MUX which takes A XNOR B as select line & the two input lines are A & Cin. Cin & A are fed to the source of PMOS and NMOS respectively. As in this case MUX is made up of two transistors.
When, A XNOR B is low, PMOS will be on and NMOS will be in off state, because of this Nmos will not conduct. As a result, Cin will be at the output as Cout. When A XNOR B is high, NMOS will be in on state and PMOS will be in off state. Now we will get A as output. In this way by using MUX, Cout is generated.

3. Simulation
The proposed full adder is made in DSCH 3.5 and it is shown below.

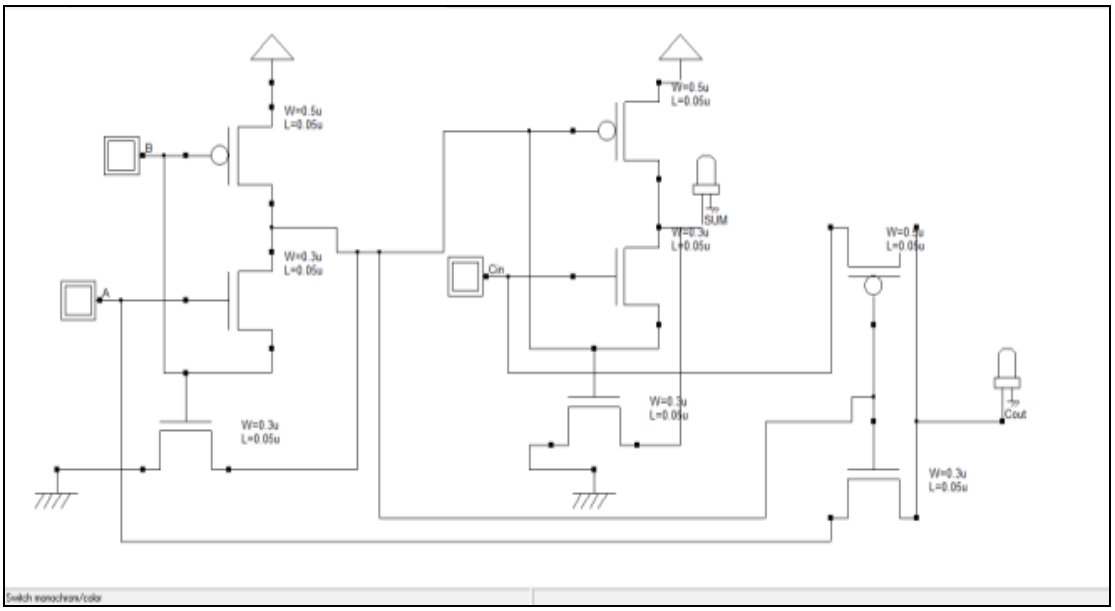

Fig 4: Schema of Full Adder in DSCH 3.5

By using the design made in DSCH 3.5 we generated a verilog file of full adder.

Auto-Generated Layout
In Microwind 3.1, by using this verilog file auto-generated layout is obtained.

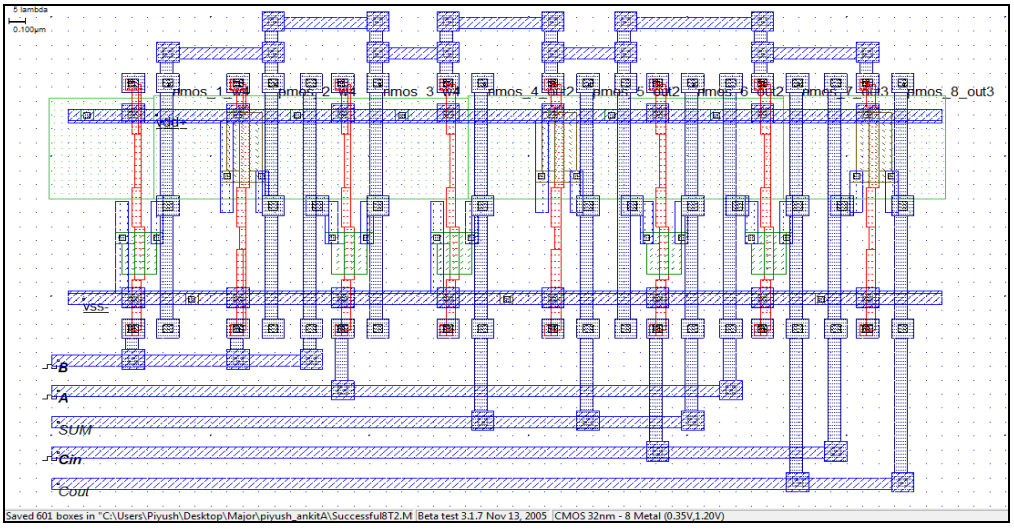

Fig 5: Auto-generated layout of 8T Full Adder

Customized Layout

Generated customized layout in Microwind 3.1 which shows variation in characteristics in comparison to the auto-generated layout.

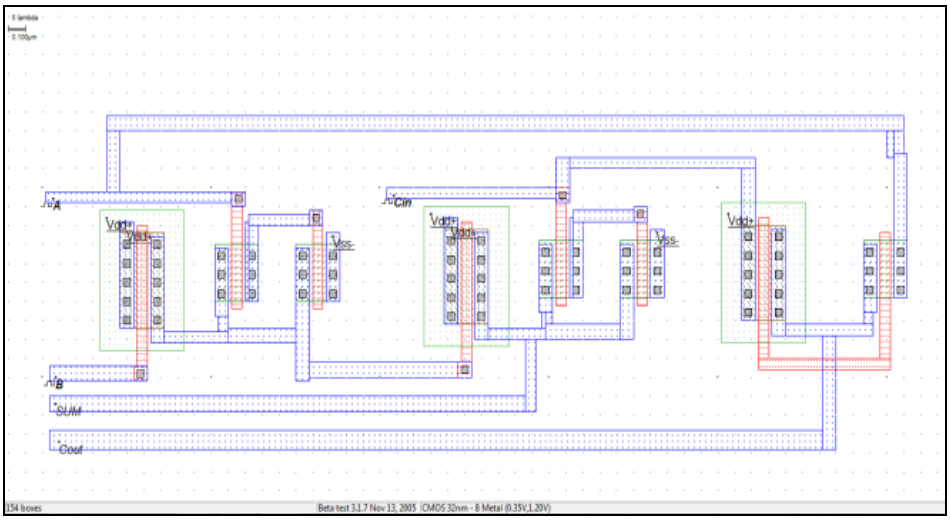

Fig 6: Customized layout of 8T Full Adder

Now from both auto generated and customized layout waveforms have been generated for inputs as well as outputs. In the figures below the simulation result is shown for the two layouts:

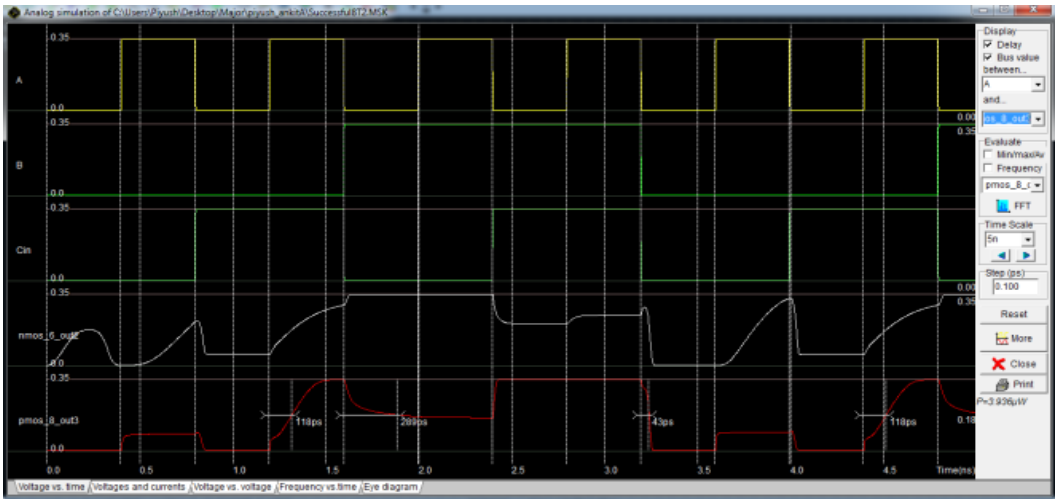

Fig 7: Analog Simulation of Auto-generated layout

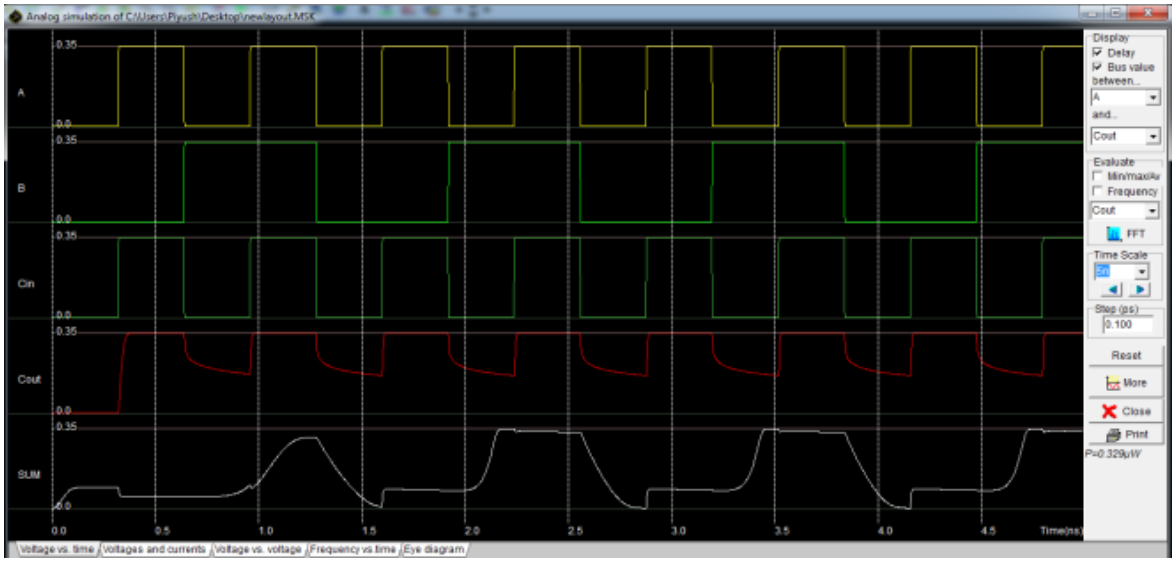

Fig 8: Analog Simulation of Customized Layout of Full Adder

4. Comparative analysis of layouts

Comparative analysis of both the layout is done on the basis of important parameters like power consumption, surf area.

Table 2: below shows the comparison of power consumption in the two layouts:

Layout Design	Power Consumption (in µW)
Auto-Generated	3.936
Customized	0.329

Customized layout also shows considerable reduction in the surf area. Comparison between the two layouts based on Surf area is shown:

Table 3

Layout Design	Surf Area (in μm^2)
Auto-Generated	19.4
Customized	9.0

In the customized layout, there is 91.64% reduction in the power consumption and 53.60% reduction in the surf area.

5. Conclusion

In this work, new design of full adder has been proposed which uses 2 XNOR gates. Two layouts of this design have been made and comparison is done between them taking parameters as power consumption and Surf area. The Customized layout shows considerable reduction in the power consumption and surf area.

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